MONOLITHIC L-BAND AMPLIFIERS OPERATING AT MILLIWATT AND SUB-MILLIWATT DC POWER CONSUMPTIONS

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ABSTRACT

A set of monolithic L-band low noise amplifiers operating at milliwatt and sub-milliwatt DC power consumptions have been designed and fabricated. A maximum gain/power quotient of 19.1 dB/mW was recorded at a frequency of 1.25 GHz with a cascade of 2 MMIC amplifiers yielding a total gain of 15.3 dB on a total power consumption of just 800 μW. This is believed to be the highest gain/power quotient ever reported for a monolithic circuit at L-band. The ultra-low power consumptions were obtained with a standard foundry process using an enhancement-mode MESFET with a variety of design techniques. Yields obtained on two 4" GaAs wafers were 96-100%.

INTRODUCTION

Minimization of DC power consumption is critical for prolonged battery life in portable RF applications. Presently, commercially available MMIC amplifier chips run at power consumptions which are an order of magnitude or more higher than what is desired for many battery operated systems. Interest in this area has been steadily increasing [1,2,5,6] because of an expanding commercial need in personal communications networks, as well as defense related applications in portable communications. Portable Global Positioning System receivers and RF tags are of interest in both the defense and commercial sectors.

DESIGN

A 1 μm MESFET process was chosen for this work because of its versatility and high reproducibility at the frequencies of interest. Since device transconductance is inversely proportional to device channel depth in the MESFET, shallower channel devices will yield improved performance at low power consumptions. For this reason, the gain potential of an enhancement-mode FET is superior to a depletion-mode FET at low current biases given similar doping profiles. This type of device has been chosen for the circuits fabricated in this work. Other authors have previously incorporated E-mode MESFETs to achieve low DC power consumptions with excellent results [2,3].

The device width must be chosen carefully in order to ensure the best circuit performance along with circuit stability and yield. Smaller width devices theoretically appear to offer higher gain for the same power consumption because of their larger transconductance at a particular power level; however, several factors degrade the performance as device width is decreased. First of all, for a constant power consumption, the device gain circles shrink as the device width is reduced, as illustrated in Fig. 1, thus requiring highly controlled element values to realize device maximum gain. Instabilities can easily result if the element values are perturbed slightly from their intended values. Secondly, the higher impedance levels of the device require higher values of matching inductance which may translate into lower inductor Qs, higher noise figures, and lower gain. In contrast, device widths which are too large will produce unacceptable small gain due to the reduced device transconductance at a fixed power level. An optimum device width can therefore be obtained by optimizing the circuit yield for a specified device gain over the frequency of interest. The optimum widths of the devices for the frequencies of interest in this work (0.9 - 1.575 GHz) were found to be between 300 and 450 μm.

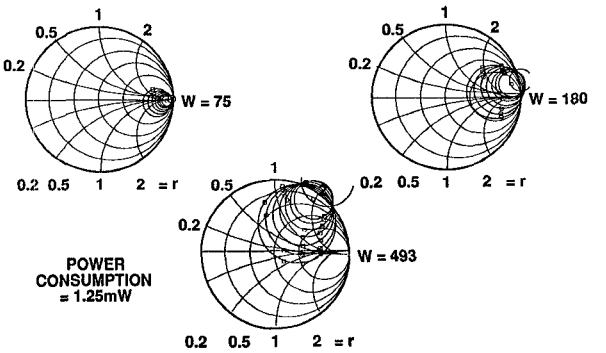

Figure 1. Gain circles for three different device widths at a constant power consumption of 1.25 mW.

Choice of device bias point is generally a tradeoff between power consumption, size, and system dynamic range and linearity requirements. In systems that do not require high linearity, the device can be operated at a point where it will yield the highest gain/power consumption. Lower gain/stage at low power consumptions will increase the number of required stages and, therefore, the amplifier size, however, the resulting reduction in the battery size may be more significant. Low power bias points may also be used in the first stages of a front end amplifier chain in a system that has higher linearity requirements so long as the overall linearity of the amplifier chain is preserved[7].

MESFETs obtain their highest gain/power efficiencies at low voltages around the "knee" (generally less than 1 V). This does not present any limitation on the use of MESFETs

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in systems with higher voltage supplies (typically 3 V to 5 V in battery powered systems) since device biasing can be easily achieved through voltage stacking (as demonstrated below) rather than current stacking as in conventional systems. The highest gain/power efficiencies for the 1.0 μm gate length enhancement-mode MESFETs used in this work were obtained at voltages of 0.5 V and current consumptions of about 0.4 mA (total device power consumption of 200 μW).

The bias network was optimized to allow sufficient temperature compensation and reasonable insensitivity to supply voltage variations. A simple resistive bias network utilizing a source resistor was found to be sufficient for these purposes.

Inductor Qs were optimized in order to realize the full potential of the minimal device gain at low power consumptions and to yield optimum noise figures. Thicker metal layers are desirable, however, when this is not an option, as with a fixed foundry process, wider line widths yield higher Qs at the expense of circuit area. This area trade-off for performance may be acceptable given the application. The measured Q's for 2 μm metal thickness lines were between 13 and 19 for the inductors designed in this work. Typical inductor widths and spacings were 20-40 μm and 5-10 μm respectively.

Two topologies, shown in Fig. 2 were used to obtain the results presented in this work. The two element matching network shown in Fig. 2a yields narrow band results, while the 3-element matching network in Fig. 2b gives a broader frequency response. The use of a source inductor is a standard low noise technique which moves the optimum noise match closer to the device conjugate match providing both excellent noise figure and input return loss.

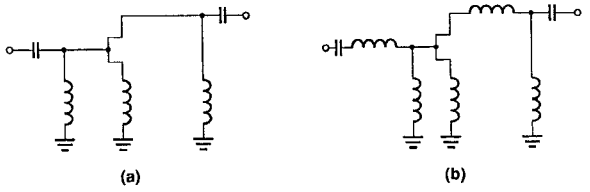


Figure 2. Circuit topologies for (a) narrowband and (b) broadband single stage amplifiers developed in this work.

RESULTS

Amplifiers were designed for several applications in the frequency range between 900 and 1575 MHz. The lumped element designs were fabricated on 25 mil 4" GaAs substrates without backmetallization. The results are plotted in Fig. 3 compared with previously published data. Table I summarizes these results. A criterion has been defined for comparison purposes as the circuit gain divided by total DC power consumption in mW. Input and output VSWRS of all of the amplifiers shown were better than 3:1 at the frequencies listed. Self-biased circuits were designed with on board variable resistances to support operation on a variety of voltage supplies and at currents correlating to the noise figure and dynamic range requirements. Yields on the circuits were generally 100% with gain variations approximately +-0.3 dB/stage across two four inch GaAs wafers.

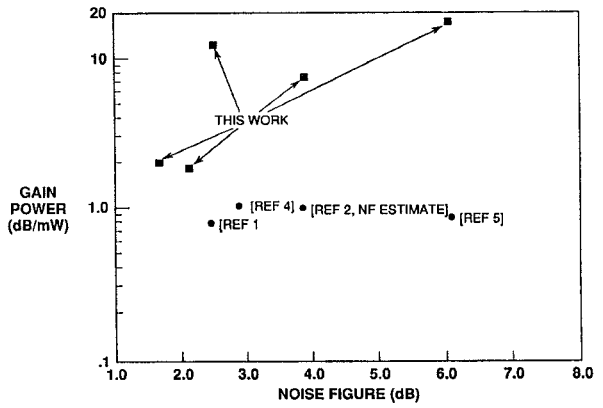


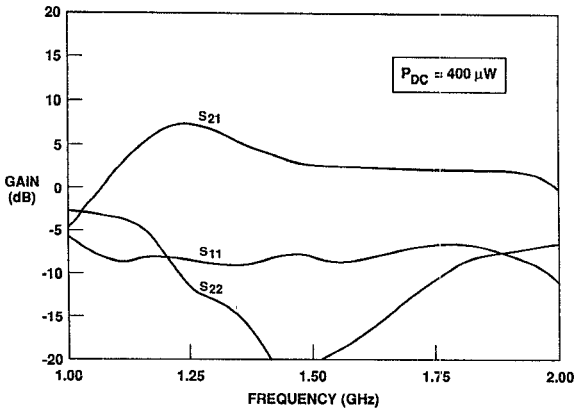
Figure 3. Comparison of the work reported here with previously published results.

CIRCUIT DESCRIPTION	FREQ (GHz)	BIAS CONDITION	P_{DC} (mW)	G (dB)	NF (dB)	SIZE (IN^2)
1 GHz LNA	1.0 1 0	2.5V @ 2mA 1V @ 0 5mA	5 0 0.5	10 3 6 0	1.6 2 5	.052x 112
1GHz SELF-BIASED NARROW-BAND 2-STAGE LNA	1.0 0 9	5V @ 2mA 2.5V @ 0.5mA	10.0 1.25	19 6 9 2	2 2 4 8	112x 112
SELF-BIASED GPS LNA	1.575 1 575	5V @ 2mA 2.5V @ 1mA	10.0 2.5	8 5 6.0	1 7 2.0	052x 112
2-STAGE AMPLIFIER	1.25	1V @ 4mA	0 41	7 2	6 0	080x 112
2-STAGE SELF-BIASED AMPLIFIER	1 25	1 5V @ 0 5mA	0 75	10.0		080x 112
SELF-BIASED GPS 2-STAGE LNA	1.575 1.575	5V @ 2mA 2 5V @ 0 5mA	10.0 1 25	17 4 9 0	2 2 3.8	080x 112
NARROW-BAND GPS LNA	1.575	2 5V @ 2mA	5.0	7 5	2.2	052x 052

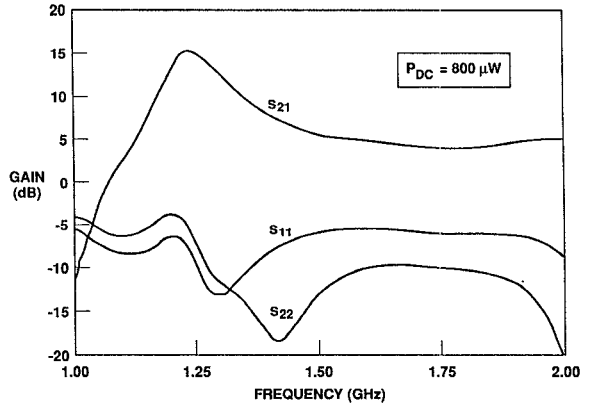
Table 1. Tabulated results for the amplifiers developed in this study.

The highest gain/power quotient was obtained on a two stage amplifier operating at 1.25 GHz on a total power consumption of 400 μW. Each of the two transistors in this amplifier were biased at 0.5 V with a current consumption of 400 μA. The gain and return loss of this amplifier are shown in Fig. 4a. A self-biased version of this amplifier operated on a single 1.5 V supply at a current consumption of 0.5 mA with a gain of about 10 dB. Both versions of the amplifier were unconditionally stable at all frequencies. The non-self-biased version was designed to be easily cascaded using voltage stacking, i.e., the MESFET source was floated. In order to demonstrate the stacking feature, a two chip cascade was assembled, the results of which are shown in Fig. 4b. In this circuit four stages are biased serially from a single 2V supply to obtain a gain of better than 15 dB on a current consumption of only 400 μA.

The lowest noise figure of 1.6 dB was obtained on a single stage amplifier which operated at 1 GHz on a total power consumption of just 5mW. This amplifier used the broadband topology shown in Fig. 2b and had a usable bandwidth between 0.7 and 1.3 GHz. This same amplifier operated at 500 μW with a noise figure of 2.5 dB and a gain of 6 dB.



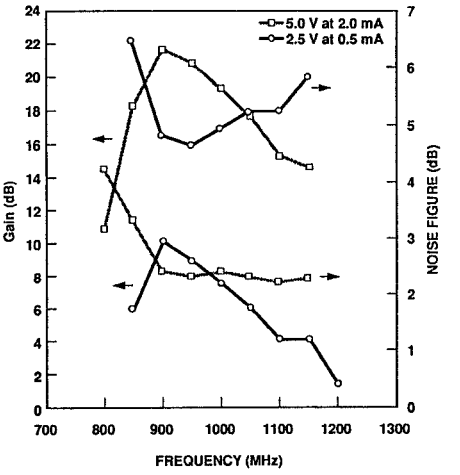
(a)



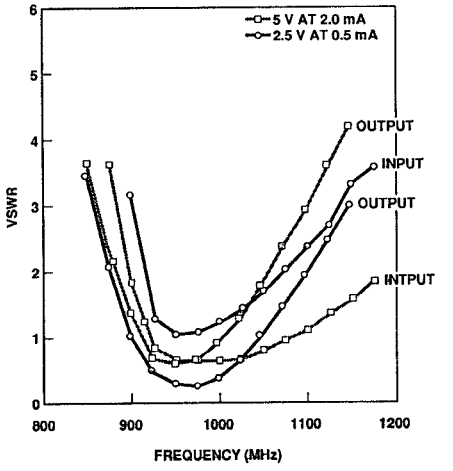
(b)

Figure 4. (a) Gain and return loss of a two-stage low power MMIC amplifier biased at 1V and 0.4mA. (b) Results for a two chip cascade of the circuit in (a) with 4 stage voltage stacking resulting in a total bias of 2V at 0.4mA.

A set of results are shown for the self-biased two stage narrowband amplifier designed for applications from .9 to 1 GHz in Figs. 5 -6. The variable bias network allowed single supply operation from a 2 V to 10 V supply and for currents from 0.5 to 5 mA. Two bias conditions 5 V @ 2 mA and 2.5 V @ 0.5 mA are shown. The circuit was unconditionally stable at all bias conditions and frequencies. As can be seen in Fig. 5c, at higher power consumptions, IP_3 results follow the rough rule of thumb of 10 dBc over the 1 dB compression point. A deviation from this rule should be expected at subthreshold currents due to the exponential dependency of the current on the gate voltage. The results in Fig. 5c indicate that IP_3 is improved relative to the 1 dB compression point at very low currents. The highest IP_3 for this circuit was 12 dBm at a power consumption of 6 V and 5 mA. Further improvements in circuit linearity at these power consumptions might be possible using devices with delta doping profiles[8]. The temperature variation of the gain and noise figure is is shown in Fig. 6 and a photo of the circuit is given in figure 7.



(a)



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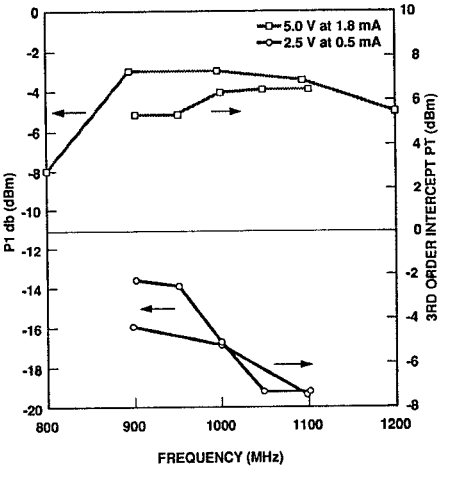

(c)

Figure 5. (a) Gain and noise figure (b) input and output VSWR and (c) 1 dB compression point and third order intercept for the 1 GHz two-stage self-biased narrowband LNA at two different bias conditions.

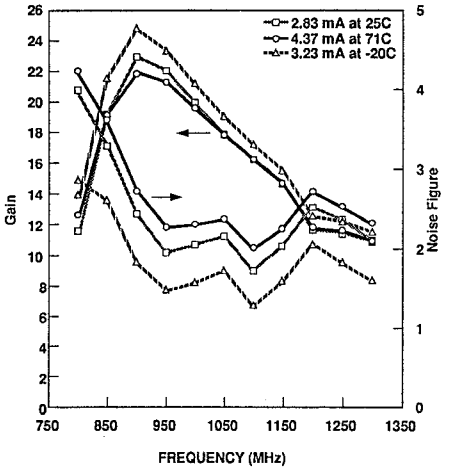

Figure 6. Gain and noise figure variation over temperature for the two-stage narrowband amplifier at a supply voltage of 6V.

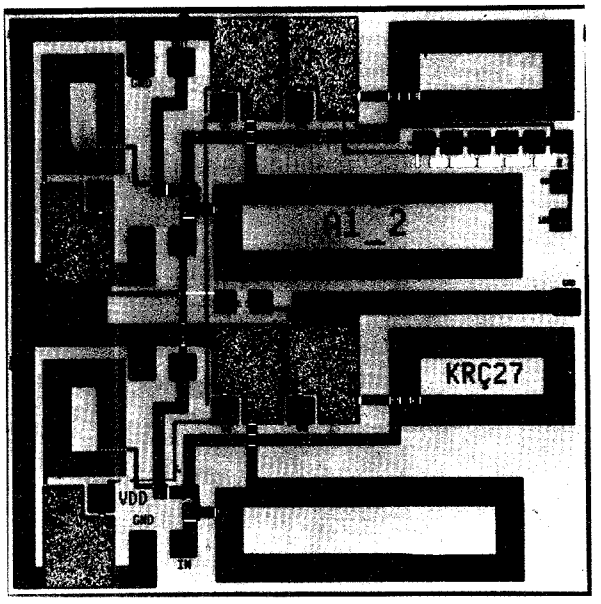

Figure 7. Photograph of the two-stage 1 GHz narrowband self-biased LNA.

A single stage version of this amplifier was also built in a self-biased configuration. Although this circuit was not as efficient in terms of power consumption, its results have been included to demonstrate statistical variation across the wafer. Figure 8 shows a simultaneous plot of the gain and input match of all of the amplifiers of this type found on a single 4" wafer. The curves in this figure were obtained by applying a single 6V supply voltage to each chip and recording the results. This type of highly repeatable performance was obtained for all of the circuits in this study.

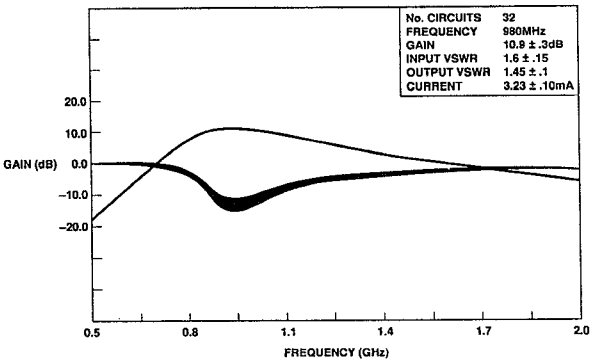

Figure 8. Statistical variation for a single stage narrowband LNA.

CONCLUSION

A set of monolithic amplifiers operating on DC power consumptions of a few milliwatts down to less than a milliwatt have been demonstrated. The amplifiers were fabricated using a standard production ready foundry process and have achieved yields approaching 100%. Power consumption reduction in MMIC components is critical for the reduction of the overall size and cost of portable RF equipment.

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